

Question 1 (3 pts): Design an encoding structure in 16-bit instruction format for the following ISA:

- 7 instructions with two addresses and one register number. $5 \times 2 = 10 \text{ bit}$
- 16 instructions with one address and one register number. 5 bit
- 10 instructions with no address and one register number. 1 bit

Suppose that an address takes up 5 bits and a register number takes 3 bits.

Question 2 (3 pts): What assembly instructions could a compiler use to implement the following code if only beq instruction is available for branching?

```

bne $s3, $s4, Else
add $s0, $s1, $s2
j Exit
Else: sub $s0, $s1, $s2
Exit:
    
```

Question 3 (2 pts): Complete the below table showing how an MIPS ALU performs the division for two unsigned integer $1000_2 / 0100_2$

Iteration	HI	LO	Divisor	Difference
0	0000	1000	0100	
1	0001	0000	0100	
2				
3				
4				

Question 4 (2 pts): What is the binary values of the signals Read register 1, Read register 2, Write register, RegDst when the instruction `addi $22, $21, -10` is processed in the below datapath? Explain your answers.

