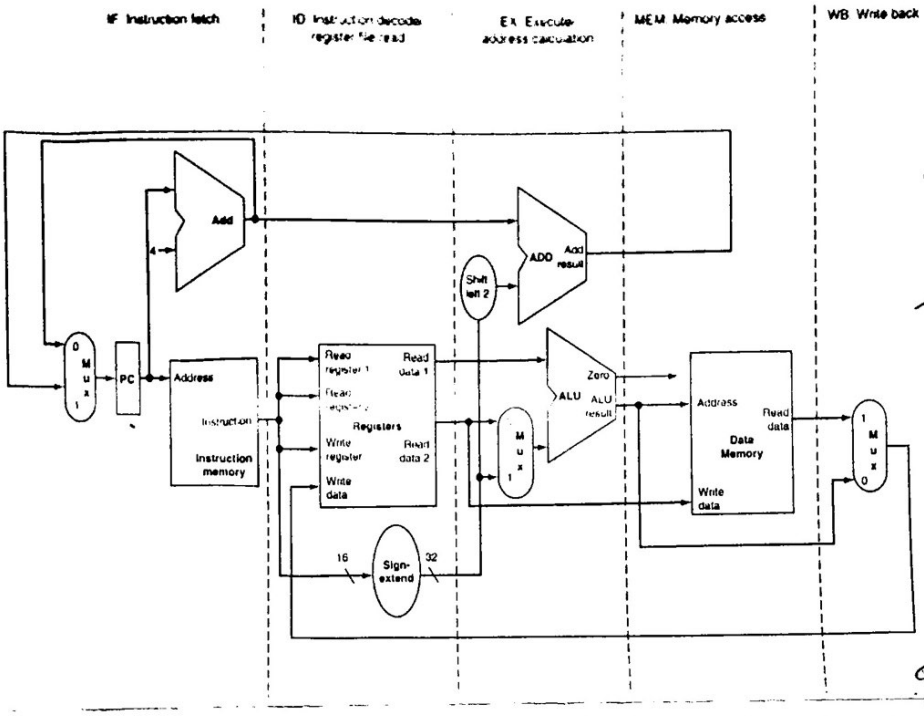
Vietnam National University, Hanoi
University of Eng. & Tech.

Course: Computer Architecture (ELT3047E)
Semester 1, 2022
Quizz 2
Duration: 20 mins



Question 1 (6 pts): Assume that the individual stages of the datapath given above have the following latencies

IF	ID	EX	MEM	WB
180ps	120ps	130ps	200ps	120ps

a. What would be the minimum clock cycle time if this datapath were **NOT** pipelined?
b. What would be the total latency of this datapath if it were pipelined?
c. If you could split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split, and what would be the total latency for the new pipeline?

Question 2 (4 pts): Assume that we execute the following code on a a 5-stage pipelined datapath given above, with the necessary interstage buffers.

```
add $t5, $t2, $t1     # 1
lw $t3, 4($t5)        # 2
lw $t2, 0($t2)        # 3
or $t3, $t5, $t3      # 4
sw $t3, 0($t5)        # 5
```

a. Identify all of the data hazards in the given sequence of instructions (state the numbers of the leading & following instructions and the register(s) involved in each data hazard)
b. Rewrite the given sequence of instructions, adding the minimal nop instructions necessary to achieve correct execution as efficiently as possible.